library ieee;

use ieee.std\_logic\_1164.all;

use ieee.std\_logic\_arith.all;

use ieee.std\_logic\_unsigned.all;

entity IC74163\_Vedant is

port

(

clk : in std\_logic;

sel : in std\_logic\_vector(3 downto 0);

l : in std\_logic\_vector(3 downto 0);

o : out std\_logic\_vector(3 downto 0)

);

end IC74163\_Vedant;

architecture IC74163\_Vedant\_arch of IC74163\_Vedant is

signal s :std\_logic\_vector(3 downto 0);

begin

process(clk,sel,l)

begin

if (clk'event and clk='0') then

if(sel(0) = '0') then

s <= "0000";

elsif(sel(1) = '0') then

s <= l;

else

if(sel = "1111") then

s <= s+1;

end if;

end if;

end if;

end process;

o <= s;

end IC74163\_Vedant\_arch;

library ieee;

use ieee.std\_logic\_1164.all;

use ieee.std\_logic\_arith.all;

use ieee.std\_logic\_unsigned.all;

entity IC74163\_Vedant\_tb is

end IC74163\_Vedant\_tb;

architecture IC74163\_Vedant\_tb\_arch of IC74163\_Vedant\_tb is

component IC74163\_Vedant is

port

(

clk : in std\_logic;

sel : in std\_logic\_vector(3 downto 0);

l : in std\_logic\_vector(3 downto 0);

o : out std\_logic\_vector(3 downto 0)

);

end component;

signal clk: std\_logic;

signal sel, l, o: std\_logic\_vector(3 downto 0);

begin

IC74163: IC74163\_Vedant port map(clk, sel, l, o);

process begin

clk <= '0';

wait for 20ns;

clk <= '1';

wait for 20ns;

end process;

process begin

sel <= "0000";

wait for 20ns;

l <= "0000";

sel <= "1000";

wait for 20ns;

sel <= "1111";

wait for 2000ns;

end process;

end IC74163\_Vedant\_tb\_arch;

